What is claimed is:

1. A structure for containing desiccant in at least one of a wafer level packaged device and a die level packaged device, the structure comprising:

a substrate;

a first metal layer disposed on the substrate within a predetermined area;

a second metal layer defining the predetermined area;

a dielectric layer disposed on the first metal layer;

a desiccant disposed on the dielectric layer;

a permeable membrane disposed on the desiccant and the dielectric layer, wherein the permeable membrane surrounds the desiccant, the dielectric layer, and the first metal layer, and is within the predetermined area; and

a plurality of metal traces disposed on the permeable membrane.

2. The structure as defined in claim 1 wherein the substrate is at least one of single crystal silicon, polycrystalline silicon, silicon oxide containing dielectric substrates, alumina, sapphire, ceramic, glass, silicon wafers, germanium wafers, gallium arsenide wafers, and mixtures thereof.

3. The structure as defined in claim 1 wherein the first metal layer, the second metal layer, and the metal traces are held substantially equi-potential to a potential of at least one of the wafer and the die.

4. The structure as defined in claim 1 wherein the first metal layer is at least one of gold, aluminum, tantalum, platinum, iridium, palladium, rhodium, nickel chromide, doped polysilicon, and mixtures thereof.

5. The structure as defined in claim 1 wherein the second metal layer is at least one of gold, aluminum, tantalum, platinum, iridium, palladium, rhodium, nickel chromide, doped polysilicon, and mixtures thereof.

6. The structure as defined in claim 1 wherein the plurality of metal traces is at least one of gold, tantalum, aluminum, platinum, iridium, palladium, rhodium, nickel chromide, and mixtures thereof.

7. The structure as defined in claim 1 wherein the dielectric layer comprises at least one of silicon oxide and silicon nitride.

8. The structure as defined in claim 1 wherein the permeable membrane comprises at least one of a polymeric material and a porous ceramic material.

9. The structure as defined in claim 8 wherein the polymeric material is a flexible material.

10. The structure as defined in claim 1 wherein the desiccant is at least one of silica gel, calcium oxide, calcium sulfate, and molecular sieves.

11. A structure for containing desiccant in a wafer level packaged device, the structure comprising:

a substrate;

a metal layer disposed on the substrate;

a permeable membrane disposed on the metal layer, the permeable membrane having a desiccant dispersed therein; and

a plurality of metal traces disposed on the permeable membrane.

12. The structure as defined in claim 11 wherein the substrate is at least one of single crystal silicon, polycrystalline silicon, silicon oxide containing dielectric substrates, alumina, sapphire, ceramic, glass, silicon wafers, germanium wafers, gallium arsenide wafers, and mixtures thereof.

13. The structure as defined in claim 11 wherein the metal layer and the plurality of metal traces are held substantially equi-potential to a potential of the wafer.

14. The structure as defined in claim 11 wherein the metal layer is at least one of gold, aluminum, tantalum, platinum, iridium, palladium, rhodium, nickel chromide, doped polysilicon, and mixtures thereof.

15. The structure as defined in claim 11 wherein the plurality of metal traces is at least one of gold, aluminum, tantalum, platinum, iridium, palladium, rhodium, nickel chromide, and mixtures thereof.

16. The structure as defined in claim 11 wherein the permeable membrane is at least one of a polymeric material and a porous ceramic material.

17. The structure as defined in claim 11 wherein the desiccant is at least one of silica gel, calcium oxide, calcium sulfate, and molecular sieves.

18. A method for making a structure for containing desiccant in at least one of a wafer level packaged device and a die level packaged device, comprising the steps of:

depositing a predetermined area-defining metal layer on a substrate;

depositing a ground plane layer within the predetermined area;

depositing a dielectric layer on the ground plane layer;

depositing a desiccant on the dielectric layer;

depositing a permeable membrane on the desiccant and the dielectric layer, wherein the permeable membrane surrounds the desiccant, the dielectric layer, and the ground plane layer, and is within the predetermined area; and

depositing a plurality of metal traces on the permeable membrane.

19. The method as defined in claim 18 wherein the depositing of the metal layer, the ground plane layer, the dielectric layer and the plurality of metal traces is accomplished by at least one of physical vapor deposition, co-sputtering, reactive sputtering, reactive co-sputtering, evaporation, pulsed laser deposition, ion beam methods, electronic-beam techniques, chemical vapor deposition, plasma enhanced chemical vapor deposition, atomic layer deposition, angle deposition, and combinations thereof.

20. The method as defined in claim 18 wherein the depositing of the permeable membrane is accomplished by at least one of spin coating, extrusion, lamination, dipping, spray coating, screen printing and chemical vapor deposition.

21. The method as defined in claim 18, further comprising the steps of:
patterning the ground plane layer;
patterning the predetermined area-defining metal layer;
patterning the dielectric layer;
patterning the desiccant;
patterning the permeable membrane; and
patterning the plurality of metal traces.

22. The method as defined in claim 21 wherein the patterning steps are accomplished by one of photolithography, photo and etch, photoresist lift-off, imprinting, and laser ablation.

23. The method as defined in claim 18 wherein the substrate is at least one of single crystal silicon, polycrystalline silicon, silicon oxide containing dielectric substrates, alumina, sapphire, ceramic, glass, silicon wafers, germanium wafers, gallium arsenide wafers, and mixtures thereof.

24. The method as defined in claim 18 wherein the predetermined-area defining metal layer and the metal traces are held substantially equi-potential to a potential of at least one of the wafer and the die.

25. A structure for containing desiccant in a wafer level packaged device produced by the process of claim 18.

26. A method for making a structure for containing desiccant in at least one of a wafer level packaged device and a die level packaged device, comprising the steps of:

depositing a metal layer on a substrate;

depositing a permeable membrane on the metal layer, the permeable membrane having a desiccant dispersed therein; and

depositing a plurality of metal traces on the permeable membrane.

27. A structure for containing desiccant in at least one of a wafer level packaged device and a die level packaged device produced by the process of claim 26.

28. The method as defined in claim 26 wherein the depositing of the metal layer and the plurality of metal traces is accomplished by physical vapor deposition, co-sputtering, reactive sputtering, reactive co-sputtering, evaporation, pulsed laser deposition, ion beam methods, electronic-beam techniques, chemical vapor deposition, plasma enhanced chemical vapor deposition, atomic layer deposition, angle deposition, and combinations thereof.

29. The method as defined in claim 26 wherein the depositing of the permeable membrane is accomplished by at least one of spin coating, extrusion, lamination, dipping, spray coating, screen printing and chemical vapor deposition.

30. The method as defined in claim 26, further comprising the step of patterning the plurality of metal traces.

31. The method as defined in claim 30 wherein the patterning step is accomplished by photolithography, photo and etch, photoresist lift-off, imprinting, and laser ablation.

32. The method as defined in claim 26 wherein the metal layer and the plurality of metal traces are held substantially equi-potential to a potential of at least one of the wafer and the die.

33. The method as defined in claim 26 wherein the desiccant is homogeneously dispersed throughout the permeable membrane.

34. An integrated circuit, comprising:

a hermetically sealed area having the integrated circuit operatively disposed therein; and

a structure within the hermetically sealed area for containing a desiccant, the structure comprising:

a substrate;

a first metal layer disposed on the substrate within a predetermined area;

a second metal layer defining the predetermined area;

a dielectric layer disposed on the first metal layer;

a desiccant disposed on the dielectric layer;

a permeable membrane disposed on the desiccant and the dielectric layer, wherein the permeable membrane surrounds the desiccant, the dielectric layer, and the first metal layer, and is within the predetermined area; and

a plurality of metal traces disposed on the permeable membrane.

35. An integrated circuit, comprising:

a hermetically sealed area having the integrated circuit operatively disposed therein; and

a structure within the hermetically sealed area for containing a desiccant, the structure comprising:

a substrate;

a metal layer disposed on the substrate;

a permeable membrane disposed on the metal layer, the permeable membrane having a desiccant dispersed therein; and

a plurality of metal traces disposed on the permeable membrane.

36. A method of using a structure for containing desiccant, the method comprising the step of:

hermetically sealing the structure for containing desiccant to a substrate having microelectronics thereon, the structure for containing desiccant comprising:

a second substrate;

a metal layer disposed on the second substrate;

a permeable membrane disposed on the metal layer, the permeable membrane having a desiccant dispersed therein; and

a plurality of metal traces disposed on the permeable membrane.

37. A hermetically sealed area, comprising:

a substrate having microelectronics thereon;

a desiccant operatively disposed within the hermetically sealed area; and

means for substantially maintaining an equipotential region around the desiccant.

38. A structure for containing desiccant in at least one of a wafer level packaged device and a die level packaged device, the structure comprising:

a substrate;

a metal layer disposed on the substrate;

a dielectric layer disposed on the metal layer;

a desiccant disposed on the dielectric layer;

a permeable membrane disposed on the desiccant and the dielectric layer, wherein the permeable membrane surrounds the desiccant, the dielectric layer, and the metal layer; and

a plurality of metal traces disposed on the permeable membrane.

39. The structure as defined in claim 38 wherein the metal layer and the metal traces are held substantially equi-potential to a potential of at least one of the wafer and the die.

40. A method for making a structure for containing desiccant in at least one of a wafer level packaged device and a die level packaged device, comprising the steps of:

depositing a metal layer on a substrate;

depositing a dielectric layer on the metal layer;

depositing a desiccant on the dielectric layer;

depositing a permeable membrane on the desiccant and the dielectric layer, wherein the permeable membrane surrounds the desiccant, the dielectric layer, and the metal layer; and

depositing a plurality of metal traces on the permeable membrane.

41. The method as defined in claim 40, further comprising the step of holding the metal layer and the metal traces at a potential that is substantially equi-potential to a potential of at least one of the wafer and the die.

42. The method as defined in claim 40 wherein the permeable membrane comprises a flexible material.

43. The method as defined in claim 42 wherein the flexible material comprises at least one of a polymeric material and a porous ceramic material.

44. The method as defined in claim 43 wherein the polymeric material comprises a photoresist comprising at least one of poly(methyl methacrylate) and photosensitive polyimide.

45. The method as defined in claim 43 wherein the porous ceramic material comprises at least one of porous aluminum oxide and porous silicon dioxide.

46. The method as defined in claim 40, further comprising the step of holding the metal layer and the metal traces at ground potential.